Software-Defined Phase-Locked Loop (PLL) Using DAHDI Timing Synchronization

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Motivation:

Reliable timing synchronization is paramount in telecommunications systems. Traditionally, this precision has relied on GPS (E1) modules, which can introduce a single point of failure, making the entire system vulnerable to disruptions, particularly in remote areas with unreliable or absent GPS signals. This project aims to develop a software-based, GPS-independent solution for robust timing synchronization using DAHDI syncronization tool as a founding stone.

Objectives:

- Goal: Develop a software-defined Phase-Locked Loop (PLL) using DAHDI to provide precise timing without GPS dependency.
- Key Aim: Create an adaptable timing solution for areas with no reliable GPS access, enhancing the performance and reliability of telecommunications.

What is a PLL?

A Phase-Locked Loop (PLL) is a control system that synchronizes an output signal's phase and frequency with a reference signal. In telecommunications, a PLL helps maintain precise timing by continuously adjusting the output to match the reference, ensuring stable and reliable signal transmission

What is DAHDI?

DAHDI and osmo-e1d: DAHDI (Digium Asterisk Hardware Device Interface) is a tool for timing control, while osmo-e1d supports the E1 protocol (GPS signal processor), commonly used in telecommunication networks

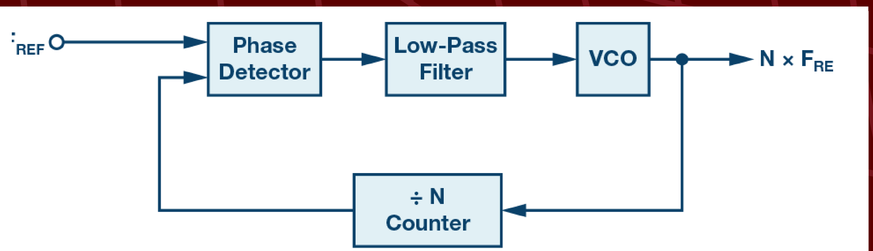

Figure 1: Basic PLL Implementation [1]

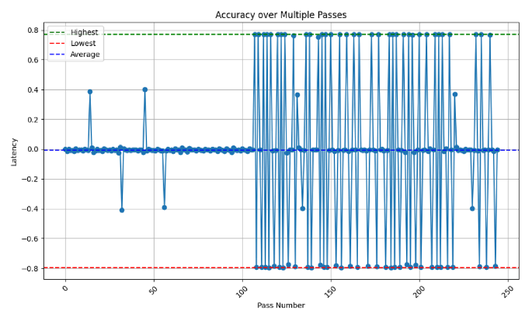

Figure 2: DAHDI tests without stabilizing mechanisms (PLL)

Methodology

- **Stage 1 - DAHDI Environment Setup:** Configure a Linux system with DAHDI compiled from Osmocom.
- **Stage 2 - Core Timer Testing:** Use dahdi_test to evaluate initial timer accuracy.
- **Stage 3 - Code Modifications:** Introduce a "fudge" field in DAHDI's timing kernel drivers to allow time adjustments.
- **Stage 4 - osmo-e1d Integration:** Run tests on filters/rules to enhance performance of such implementation

References:

[1] Ian Collins. (2018). *Analog Dialogue 52-07*. https://www.analog.com/media/en/analog-dialogue/volume-52/number-3/phase-locked-loop-pll-fundamentals.pdf